ABSTRACT OF THE DISCLOSURE

[0043] A memory control apparatus and method for digital signal processing capable of operating with a plurality of digital signal processors (DSPs) using a single memory slot and a buffer. The apparatus includes at least one DSP for processing different signals, a flash memory which can record and reproduce a digital signal, a plurality of selection switches, located on signal lines between the DSP and the flash memory, for switching input/output of signals, a three-state buffer which selectively outputs insert information of the flash memory to the DSPs according to a control signal, a control unit for providing the control signal for controlling switching of the signals, and a key input unit for determining input/output operation modes. The control unit records or reproduces the data in the flash memory according to the operation mode determined through the key input unit. The memory and the buffer are commonly used when a plurality of DSPs are operated, and thus an operation system having a simple construction is provided.